MT6739CH LTE Smartphone Application Processor Technical Brief

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Document Revision History

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

MT6739CH device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE smart phone applications,. The chip integrates Quad-core ARM® Cortex-A53 operating up to 1.5 GHz, an Imagination MIPS32® InterAptive processor and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Quad-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games.
All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

An Imagination MIPS32® InterAptive processor, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 4, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE. Supports CDMA2000 HRPD/1xEV-DO Revision 0 and A (3.1Mbps for forward link and 1.8Mbps for reverse link).

MT6739CH also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6739CH provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6739CH

- Quad-core ARM® Cortex-A53 MPCore™ operating at 1.5GHz
- LPDDR3 up to 3GB, 667MHz
- LTE Cat 4 (150Mbps)
- CDMA2000 HRPD/1xEV-DO Revision 0 and A.
- HPUE
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to HD+ (1440*720 60 fps)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 13MP@30fps.
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR ,EVS)

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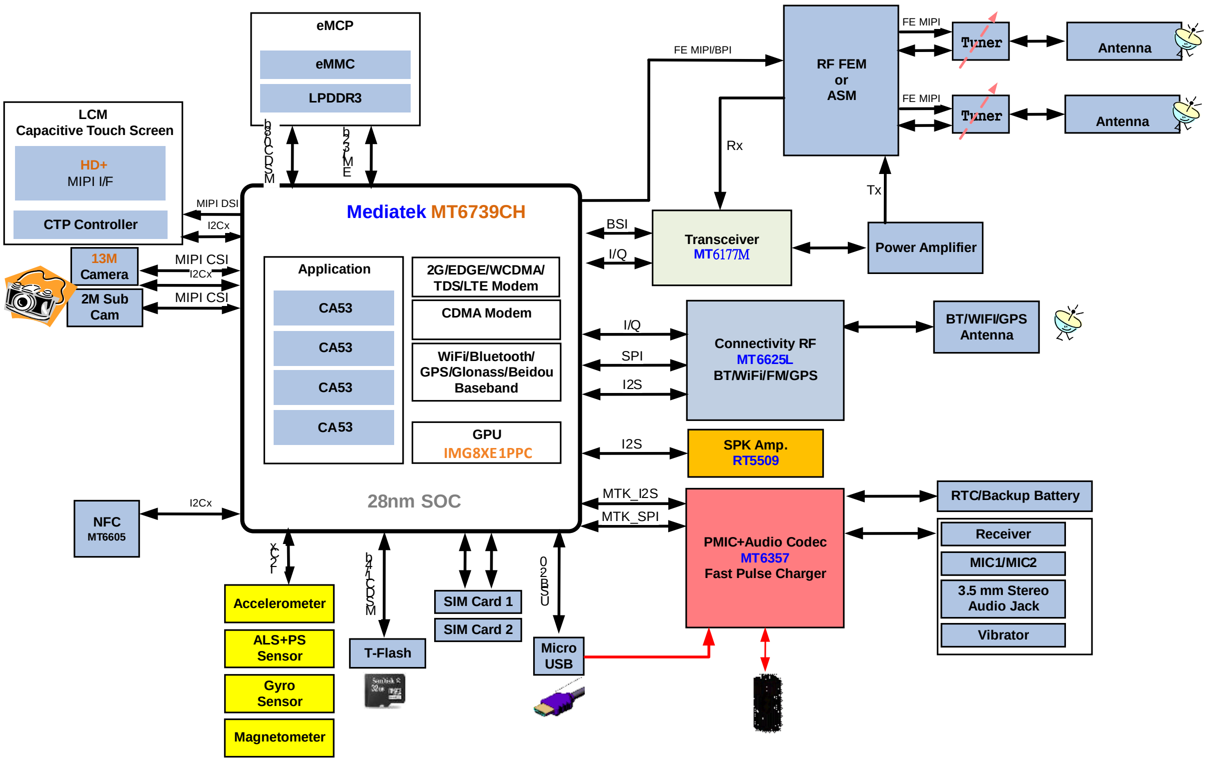

Figure 1-1. High-level MT6739CH functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - eMMC boot support
  - Supports LPDDR-3

- **AP MCU subsystem**
  - Four-core ARM® Cortex-A53 MPCore™ operating at 1.5GHz
  - Supports ARMv8-A architecture for both 32 and 64-bit execution state
  - Supports NEON multimedia processing engine with SIMDv2/VFPv4 ISA
  - Optimal support ARMv8 Cryptographic extension
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 256KB unified L2 cache for CPU cluster

- **MD MCU subsystem**
  - Imagination MIPS32® InterAptive processor with max. 600 MHz operation frequency
  - High-performance Multi-core and Multi-thread processor architecture(Two cores and two threads)
  - 32KB L1 I-cache and 32KB L1 D-cache per core
  - 384KB SPRAM (Scratchpad memory, Two-Core's ISPRAM and DSPRAM)
  - 256KB L2 Cache (Share L2 cache for two cores)
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security
  - Hardware Crypto Engine support

- **External memory interface**
  - LPDDR3 up to 3GB
  - Single channel with 32-bit data bus width
  - Memory clock up to 667MHz
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 HS/FS support
  - eMMC5.1
  - 2 UART for debugging and applications
  - 3 SPI master for external devices
  - 6 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 5 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 1 set of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO3.0 protocols

- **Operating conditions**
  - Core voltage: 1.15V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: VFBGA
  - 11.8mm*11.0mm
  - Height: Max. 0.9mm

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- Ball count: 491 balls
- Ball pitch: 0.4mm

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1.3 Modem Features

- **LTE**
  - FDD/TDD: Up to 150Mbps downlink, 50Mbps uplink
  - 1.4 to 20MHz RF bandwidth
  - 2*2 downlink SU-MIMO; 4*2 downlink SU-MIMO
  - IPv6, QoS
  - Inter-RAT capabilities with HSPA+, EDGE and applicable backward-compatible modes
  - SNOW3G/ZUC cipher offload engine
  - HPUE

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2, A5/3 and A5/4 ciphering
  - GPRS GEA1, GEA2, GEA3 and GEA4 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology
  - VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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- **CDMA2000**
  - Supports CDMA2000 1xRTT (release 0 and Advanced) and CDMA2000 HRPD/1xEV-DO Revision 0 and A.
  - Hybrid operation between 1x and HRPD
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link.
  - Supports 1x Diversity.

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1.4 Connectivity Features

MT6739CH includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625L. With four advanced radio technologies integrated on one chip, MT6739CH/MT6625L is the best and most convenient connectivity solution in the industry, MT6739CH implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4 GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Dual-band (2.4GHz/5GHz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.2 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 5 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality

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- Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - GPS/Glonass/Beidou/QZSS
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 8dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBµVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up HD+(1440*720 60 fps)
  - MIPI DSI interface (4 data lanes)
  - DBI interface (9-bit/HVGA@30fps)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Single and dual antenna operation, spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling

- **Graphics**
  - 3D graphic accelerator capable of processing up to 142M tri/sec and 570M pixel/sec and 9.1Gflops @ 570 MHz
  - Support API standards OpenGL ES 1.1/2.0/3.0/3.2, OpenCL 1.0/1.1/1.2 EP and DirectX9

- **Image**
  - Integrated image signal processor supports 13MP@30fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 13M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - Hardware JPEG encoder: Baseline encoding with 130M pixel/sec. Continuous shot with 96M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM
  - External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
  - 4-band IIR compensation filter to enhance loudspeaker responses

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- Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
- Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR, EVS)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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1.6 General Description

MediaTek's MT6739CH is a highly integrated LTE System-on-Chip (SoC) which incorporates advanced features, e.g. LTE cat.4, 3D graphics (OpenGL|ES 3.0), 13M camera ISP, LPDDR3-667MHz, HD+ display and 1080p video codec. MT6739CH helps phone manufacturers build high-performance LTE smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!

Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6739CH is the brand-new generation smart phone SoC integrating MediaTek LTE modem, Quad-core ARM® Cortex-A53 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-value Product!

To enrich camera features, MT6739CH equips a 13M camera ISP with advanced features, e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, panorama view, picture in picture, video in video and video face beautication.

Incredible Browser Experience!

The powerful CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeping low standby power. GPU supporting OpenGL|ES 3.0 also provides you with excellent multimedia experiences.

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

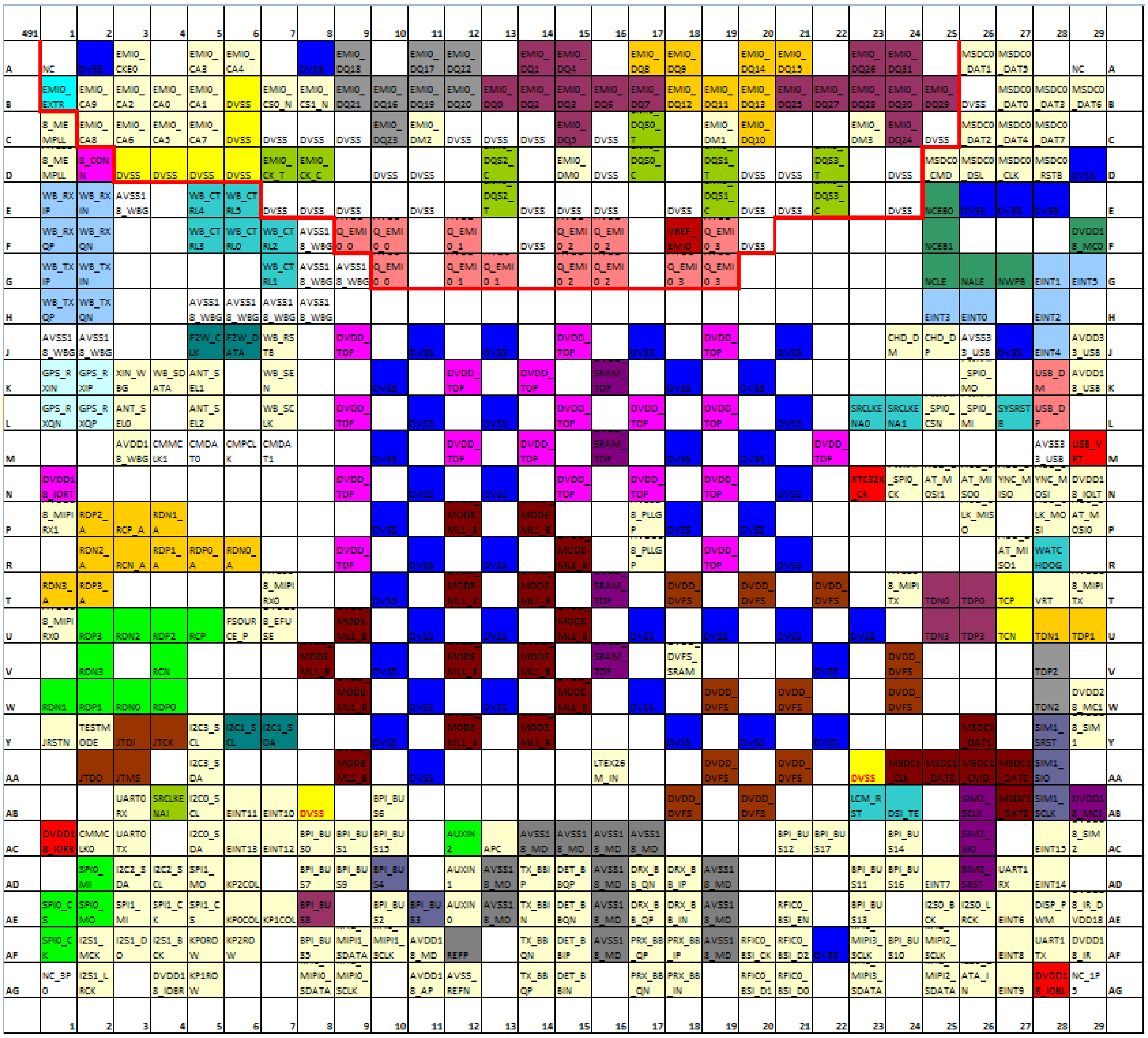

Figure 2-1. Ball map view

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2.1.2 Pin Coordinate

Table 2-1. Pin coordinate (using LPDDR3)

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	J1	AVSS18_WBG	W21	DVDD_DVFS
A2	DVSS	J2	AVSS18_WBG	W24	DVDD_DVFS
A3	EMI0_CKE0	J5	F2W_CLK	W28	TDN2
A5	EMI0_CA3	J6	F2W_DATA	W29	DVDD28_MC1
A6	EMI0_CA4	J7	WB_RSTB	Y1	JRSTN
A8	DVSS	J9	DVDD_TOP	Y2	TESTMODE
A9	EMI0_DQ18	J11	DVSS	Y3	JTDI
A11	EMI0_DQ17	J13	DVSS	Y4	JTCK
A12	EMI0_DQ22	J15	DVDD_TOP	Y5	I2C3_SCL
A14	EMI0_DQ1	J17	DVSS	Y6	I2C1_SCL
A15	EMI0_DQ4	J19	DVDD_TOP	Y7	I2C1_SDA
A17	EMI0_DQ8	J21	DVSS	Y10	DVSS
A18	EMI0_DQ9	J24	CHD_DM	Y12	DVDD_MODEML1_BUCK
A20	EMI0_DQ14	J25	CHD_DP	Y14	DVDD_MODEML1_BUCK
A21	EMI0_DQ15	J26	AVSS33_USB	Y18	DVSS
A23	EMI0_DQ26	J27	DVSS	Y20	DVSS
A24	EMI0_DQ31	J28	EINT4	Y22	DVSS
A26	MSDC0_DAT1	J29	AVDD33_USB	Y26	MSDC1_DAT1
A27	MSDC0_DAT5	K1	GPS_RXIN	Y28	SIM1_SRST
A29	NC	K2	GPS_RXIP	Y29	DVDD28_SIM1
B1	EMI0_EXTR	K3	XIN_WBG	AA2	JTDO
B2	EMI0_CA9	K4	WB_SDATA	AA3	JTMS
B3	EMI0_CA2	K5	ANT_SEL1	AA5	I2C3_SDA
B4	EMI0_CA0	K7	WB_SEN	AA9	DVDD_MODEML1_BUCK
B5	EMI0_CA1	K10	DVSS	AA11	DVSS
B6	DVSS	K12	DVDD_TOP	AA16	LTEX26M_IN
B7	EMI0_CS0_N	K14	DVDD_TOP	AA19	DVDD_DVFS
B8	EMI0_CS1_N	K16	DVDD_SRAM_TOP	AA21	DVDD_DVFS
B9	EMI0_DQ21	K18	DVSS	AA23	DVSS
B10	EMI0_DQ16	K20	DVSS	AA24	MSDC1_CLK
B11	EMI0_DQ19	K26	PWRAP_SPI0_MO	AA25	MSDC1_DAT3
B12	EMI0_DQ20	K28	USB_DM	AA26	MSDC1_CMD
B13	EMI0_DQ0	K29	AVDD18_USB	AA27	MSDC1_DAT0
B14	EMI0_DQ2	L1	GPS_RXQN	AA28	SIM1_SIO
B15	EMI0_DQ3	L2	GPS_RXQP	AB3	UART0RX
B16	EMI0_DQ6	L3	ANT_SEL0	AB4	SRCLKENAI
B17	EMI0_DQ7	L5	ANT_SEL2	AB5	I2C0_SCL

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
B18	EMI0_DQ12	L7	WB_SCLK	AB6	EINT11
B19	EMI0_DQ11	L9	DVDD_TOP	AB7	EINT10
B20	EMI0_DQ13	L11	DVSS	AB8	DVSS
B21	EMI0_DQ25	L13	DVSS	AB10	BPI_BUS6
B22	EMI0_DQ27	L15	DVDD_TOP	AB18	DVDD_DVFS
B23	EMI0_DQ28	L17	DVDD_TOP	AB20	DVDD_DVFS
B24	EMI0_DQ30	L19	DVDD_TOP	AB23	LCM_RST
B25	EMI0_DQ29	L21	DVSS	AB24	DSI_TE
B26	DVSS	L23	SRCLKENA0	AB26	SIM2_SCLK
B27	MSDC0_DAT0	L24	SRCLKENA1	AB27	MSDC1_DAT2
B28	MSDC0_DAT3	L25	PWRAP_SPI0_CSN	AB28	SIM1_SCLK
B29	MSDC0_DAT6	L26	PWRAP_SPI0_MI	AB29	DVDD18_MC1
C1	AVDD18_MEMPLL	L27	SYSRSTB	AC1	DVDD18_IORB
C2	EMI0_CA8	L28	USB_DP	AC2	CMMCLK0
C3	EMI0_CA6	M3	AVDD18_WBG	AC3	UART0TX
C4	EMI0_CA5	M4	CMMCLK1	AC5	I2C0_SDA
C5	EMI0_CA7	M5	CMDAT0	AC6	EINT13
C6	DVSS	M6	CMPCLK	AC7	EINT12
C7	DVSS	M7	CMDAT1	AC8	BPI_BUS0
C8	DVSS	M10	DVSS	AC9	BPI_BUS1
C9	DVSS	M12	DVDD_TOP	AC10	BPI_BUS15
C10	EMI0_DQ23	M14	DVDD_TOP	AC12	AUXIN2
C11	EMI0_DM2	M16	DVDD_SRAM_TOP	AC13	APC
C12	DVSS	M18	DVSS	AC14	AVSS18_MD
C13	DVSS	M20	DVSS	AC15	AVSS18_MD
C14	DVSS	M22	DVDD_TOP	AC16	AVSS18_MD
C15	EMI0_DQ5	M28	AVSS33_USB	AC17	AVSS18_MD
C16	DVSS	M29	USB_VRT	AC21	BPI_BUS12
C17	EMI0_DQS0_T	N1	DVDD18_IORT	AC22	BPI_BUS17
C19	EMI0_DM1	N9	DVDD_TOP	AC24	BPI_BUS14
C20	EMI0_DQ10	N11	DVSS	AC26	SIM2_SIO
C23	EMI0_DM3	N13	DVSS	AC28	EINT15
C24	EMI0_DQ24	N15	DVDD_TOP	AC29	DVDD28_SIM2
C25	DVSS	N17	DVDD_TOP	AD2	SPI0_MI
C26	MSDC0_DAT2	N19	DVDD_TOP	AD3	I2C2_SDA
C27	MSDC0_DAT4	N21	DVSS	AD4	I2C2_SCL
C28	MSDC0_DAT7	N23	RTC32K_CK	AD5	SPI1_MO
D1	AVSS18_MEMPLL	N24	PWRAP_SPI0_CK	AD6	KP2COL
D2	DVDD18_CONN	N25	AUD_DAT_MOSI1	AD8	BPI_BUS7
D3	DVSS	N26	AUD_DAT_MISO0	AD9	BPI_BUS9
D4	DVSS	N27	AUD_SYNC_MISO	AD10	BPI_BUS4
D5	DVSS	N28	AUD_SYNC_MOSI	AD12	AUXIN1
D6	DVSS	N29	DVDD18_IOLT	AD13	AVSS18_MD

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
D7	EMI0_CK_T	P1	AVDD18_MIPIRX1	AD14	TX_BBIP
D8	EMI0_CK_C	P2	RDP2_A	AD15	DET_BBQP
D10	DVSS	P3	RCP_A	AD16	AVSS18_MD
D11	DVSS	P4	RDN1_A	AD17	DRX_BB_QN
D13	EMI0_DQS2_C	P10	DVSS	AD18	DRX_BB_IP
D15	EMI0_DM0	P12	DVDD_MODEML1_BUCK	AD19	AVSS18_MD
D16	DVSS	P14	DVDD_MODEML1_BUCK	AD23	BPI_BUS11
D17	EMI0_DQS0_C	P17	AVSS18_PLLGP	AD24	BPI_BUS16
D19	EMI0_DQS1_T	P18	DVSS	AD25	EINT7
D20	DVSS	P20	DVSS	AD26	SIM2_SRST
D21	DVSS	P26	AUD_CLK_MISO	AD27	UART1RX
D22	EMI0_DQS3_T	P28	AUD_CLK_MOSI	AD28	EINT14
D24	DVSS	P29	AUD_DAT_MOSI0	AE1	SPI0_CS
D25	MSDC0_CMD	R2	RDN2_A	AE2	SPI0_MO
D26	MSDC0_DSL	R3	RCN_A	AE3	SPI1_MI
D27	MSDC0_CLK	R4	RDP1_A	AE4	SPI1_CK
D28	MSDC0_RSTB	R5	RDP0_A	AE5	SPI1_CS
D29	DVSS	R6	RDN0_A	AE6	KP0COL
E1	WB_RXIP	R9	DVDD_TOP	AE7	KP1COL
E2	WB_RXIN	R11	DVSS	AE8	BPI_BUS8
E3	AVSS18_WBG	R13	DVSS	AE10	BPI_BUS2
E5	WB_CTRL4	R15	DVDD_MODEML1_BUCK	AE11	BPI_BUS3
E6	WB_CTRL5	R17	AVDD18_PLLGP	AE12	AUXIN0
E7	DVSS	R19	DVDD_TOP	AE13	AVSS18_MD
E8	DVSS	R21	DVSS	AE14	TX_BBIN
E9	DVSS	R27	AUD_DAT_MISO1	AE15	DET_BBQN
E11	DVSS	R28	WATCHDOG	AE16	AVSS18_MD
E13	EMI0_DQS2_T	T1	RDN3_A	AE17	DRX_BB_QP
E14	DVSS	T2	RDP3_A	AE18	DRX_BB_IN
E15	DVSS	T7	AVSS18_MIPIRX0	AE19	AVSS18_MD
E16	DVSS	T10	DVSS	AE21	RFIC0_BSI_EN
E18	DVSS	T12	DVDD_MODEML1_BUCK	AE23	BPI_BUS13
E19	EMI0_DQS1_C	T14	DVDD_MODEML1_BUCK	AE25	I2S0_BCK
E20	DVSS	T16	DVDD_SRAM_TOP	AE26	I2S0_LRCK
E21	DVSS	T18	DVDD_DVFS	AE27	EINT6
E22	EMI0_DQS3_C	T20	DVDD_DVFS	AE28	DISP_PWM
E24	DVSS	T22	DVDD_DVFS	AE29	DVDD28_IR_DVDD18_EINT
E25	NCEB0	T24	AVSS18_MIPITX	AF1	SPI0_CK

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
E26	DVSS	T25	TDN0	AF2	I2S1_MCK
E27	DVSS	T26	TDP0	AF3	I2S1_DO
E28	DVSS	T27	TCP	AF4	I2S1_BCK
F1	WB_RXQP	T28	VRT	AF5	KP0ROW
F2	WB_RXQN	T29	AVDD18_MIPITX	AF6	KP2ROW
F5	WB_CTRL3	U1	AVDD18_MIPIRX0	AF8	BPI_BUS5
F6	WB_CTRL0	U2	RDP3	AF9	RFIC_MIPI1_SDATA
F7	WB_CTRL2	U3	RDN2	AF10	RFIC_MIPI1_SCLK
F8	AVSS18_WBG	U4	RDP2	AF11	AVDD18_MD
F9	AVDDQ_EMI0_0	U5	RCP	AF12	REFP
F10	AVDDQ_EMI0_0	U6	FSOURCE_P	AF14	TX_BBQN
F12	AVDDQ_EMI0_1	U7	DVDD18_EFUSE	AF15	DET_BBIP
F14	DVSS	U9	DVDD_MODEML1_BUCK	AF16	AVSS18_MD
F15	AVDDQ_EMI0_2	U11	DVSS	AF17	PRX_BB_QP
F16	AVDDQ_EMI0_2	U13	DVSS	AF18	PRX_BB_IP
F18	VREF_EMI0	U15	DVDD_MODEML1_BUCK	AF19	AVSS18_MD
F19	AVDDQ_EMI0_3	U17	DVSS	AF20	RFIC0_BSI_CK
F20	DVSS	U19	DVSS	AF21	RFIC0_BSI_D2
F25	NCEB1	U21	DVSS	AF22	DVSS
F29	DVDD18_MC0	U23	DVSS	AF23	RFIC_MIPI3_SCLK
G1	WB_TXIP	U25	TDN3	AF24	BPI_BUS10
G2	WB_TXIN	U26	TDP3	AF25	RFIC_MIPI2_SCLK
G7	WB_CTRL1	U27	TCN	AF27	EINT8
G8	AVSS18_WBG	U28	TDN1	AF28	UART1TX
G9	AVSS18_WBG	U29	TDP1	AF29	DVDD18_IR
G10	AVDDQ_EMI0_0	V2	RDN3	AG1	NC_3P0
G12	AVDDQ_EMI0_1	V4	RCN	AG2	I2S1_LRCK
G13	AVDDQ_EMI0_1	V8	DVDD_MODEML1_BUCK	AG4	DVDD18_IOBR
G15	AVDDQ_EMI0_2	V10	DVSS	AG5	KP1ROW
G16	AVDDQ_EMI0_2	V12	DVDD_MODEML1_BUCK	AG8	RFIC_MIPI0_SDATA
G18	AVDDQ_EMI0_3	V14	DVDD_MODEML1_BUCK	AG9	RFIC_MIPI0_SCLK
G19	AVDDQ_EMI0_3	V16	DVDD_SRAM_TOP	AG11	AVDD18_AP
G25	NCLE	V18	DVDD_DVFS_SRAM	AG12	AVSS_REFN
G26	NALE	V22	DVSS	AG14	TX_BBQP
G27	NWPB	V24	DVDD_DVFS	AG15	DET_BBIN
G28	EINT1	V28	TDP2	AG17	PRX_BB_QN
G29	EINT5	W1	RDN1	AG18	PRX_BB_IN
H1	WB_TXQP	W2	RDP1	AG20	RFIC0_BSI_D1

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
H2	WB_TXQN	W3	RDN0	AG21	RFIC0_BSI_D0
H5	AVSS18_WBG	W4	RDP0	AG23	RFIC_MIPI3_SDATA
H6	AVSS18_WBG	W9	DVDD_MODEML1_BUCK	AG25	RFIC_MIPI2_SDATA
H7	AVSS18_WBG	W11	DVSS	AG26	I2S0_DATA_IN
H8	AVSS18_WBG	W13	DVSS	AG27	EINT9
H25	EINT3	W15	DVDD_MODEML1_BUCK	AG28	DVDD18_IOBL
H26	EINT0	W17	DVSS	AG29	NC_1P5
H28	EINT2	W19	DVDD_DVFS		

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-3. Detailed pin description (using LPDDR3)

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DI	System reset input	DVDD18_IOLT
WATCHDOG	DO	Watchdog reset output	DVDD18_IOLT
TESTMODE	DIO	Test mode	DVDD18_IORB
RTC32K_CK	DIO	32K clock input	DVDD18_IOLT
SRCLKENAI	DIO	26MHz co-clock enable input	DVDD18_IORB
SRCLKENA0	DIO	26MHz co-clock enable output	DVDD18_IOLT
SRCLKENA1	DIO	26MHz co-clock enable output	DVDD18_IOLT
PMIC			
PWRAP_SPI0_MO	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_MI	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CSN	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CK	DIO	PMIC SPI control interface	DVDD18_IOLT
AUD_CLK_MISO	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_CLK_MOSI	DIO	PMIC audio input interface	DVDD18_IOLT

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Pin name	Type	Description	Power domain
AUD_SYNC_MISO	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_SYNC_MOSI	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MOSI0	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MOSI1	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MISO0	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MISO1	DIO	PMIC audio input interface	DVDD18_IOLT
SIM			
SIM1_SIO	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	DIO	SIM1 reset, PMIC interface	DVDD28_SIM1
SIM1_SCLK	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM2_SIO	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SRST	DIO	SIM2 reset, PMIC interface	DVDD28_SIM2
SIM2_SCLK	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
JTAG			
JTCK	DIO	JTCK	DVDD18_IORB
JTDO	DIO	JTDO	DVDD18_IORB
JTDI	DIO	JTDI	DVDD18_IORB
JTMS	DIO	JTMS	DVDD18_IORB
JRSTN	DIO	JRSTN	DVDD18_IORB
LCD			
DISP_PWM	DIO	Display PWM output	DVDD18_IOBL
DSI_TE	DIO	Parallel display interface tearing effect	DVDD18_IOBL
LCM_RST	DIO	Parallel display interface reset signal	DVDD18_IOBL
I2S			
I2S0_DATA_IN	DIO	I2S0 data input pin	DVDD18_IOBL
I2S0_BCK	DIO	I2S0 clock	DVDD18_IOBL
I2S0_LRCK	DIO	I2S0 word select	DVDD18_IOBL
I2S1_BCK	DIO	I2S1_BCK	DVDD18_IOBR
I2S1_DO	DIO	I2S1_DO	DVDD18_IOBR
I2S1_LRCK	DIO	I2S1_LRCK	DVDD18_IOBR
I2S1_MCK	DIO	I2S1_MCK	DVDD18_IOBR
EINT			
EINT0	DIO	External interrupt 0	DVDD18_MC0
EINT1	DIO	External interrupt 1	DVDD18_MC0
EINT2	DIO	External interrupt 2	DVDD18_MC0
EINT3	DIO	External interrupt 3	DVDD18_MC0
EINT4	DIO	External interrupt 4	DVDD18_MC0
EINT5	DIO	External interrupt 5	DVDD18_MC0
EINT6	DIO	External interrupt 6	DVDD18_IOBL
EINT7	DIO	External interrupt 7	DVDD18_IOBL
EINT8	DIO	External interrupt 8	DVDD18_IOBL

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Pin name	Type	Description	Power domain
EINT9	DIO	External interrupt 9	DVDD18_IOBL
EINT10	DIO	External interrupt 10	DVDD18_IORB
EINT11	DIO	External interrupt 11	DVDD18_IORB
EINT12	DIO	External interrupt 12	DVDD18_IOBR
EINT13	DIO	External interrupt 13	DVDD18_IOBR
EINT14	DIO	External interrupt 14	DVDD28_IR_DVDD18_EINT
EINT15	DIO	External interrupt 15	DVDD28_IR_DVDD18_EINT
UART			
UART0RX	DIO	UART0 RX	DVDD18_IORB
UART0TX	DIO	UART0 TX	DVDD18_IORB
UART1RX	DIO	UART1 RX	DVDD18_IOBL
UART1TX	DIO	UART1 TX	DVDD18_IOBL
SPI			
SPI0_CS	DIO	SPI0 chip select	DVDD18_IORB
SPI0_CK	DIO	SPI0 data in	DVDD18_IORB
SPI0_MI	DIO	SPI0 data out	DVDD18_IORB
SPI0_MO	DIO	SPI0 clock	DVDD18_IORB
SPI1_CS	DIO	SPI1 chip select	DVDD18_IOBR
SPI1_CK	DIO	SPI1 data in	DVDD18_IOBR
SPI1_MI	DIO	SPI1 data out	DVDD18_IOBR
SPI1_MO	DIO	SPI1 clock	DVDD18_IOBR
BPI			
BPI_BUS0	DIO	BPI1 BUS0	DVDD18_IOBR
BPI_BUS1	DIO	BPI1 BUS1	DVDD18_IOBR
BPI_BUS2	DIO	BPI1 BUS2	DVDD18_IOBR
BPI_BUS3	DIO	BPI1 BUS3	DVDD18_IOBR
BPI_BUS4	DIO	BPI1 BUS4	DVDD18_IOBR
BPI_BUS5	DIO	BPI1 BUS5	DVDD18_IOBR
BPI_BUS6	DIO	BPI1 BUS6	DVDD18_IOBR
BPI_BUS7	DIO	BPI1 BUS7	DVDD18_IOBR
BPI_BUS8	DIO	BPI1 BUS8	DVDD18_IOBR
BPI_BUS9	DIO	BPI1 BUS9	DVDD18_IOBR
BPI_BUS10	DIO	BPI1 BUS10	DVDD18_IOBL
BPI_BUS11	DIO	BPI1 BUS11	DVDD18_IOBL
BPI_BUS12	DIO	BPI1 BUS12	DVDD18_IOBL
BPI_BUS13	DIO	BPI1 BUS13	DVDD18_IOBL
BPI_BUS14	DIO	BPI1 BUS14	DVDD18_IOBL
BPI_BUS15	DIO	BPI1 BUS15	DVDD18_IOBR
BPI_BUS16	DIO	BPI1 BUS16	DVDD18_IOBL
BPI_BUS17	DIO	BPI1 BUS17	DVDD18_IOBL
ANT_SEL0	DIO	Antenna select 0	DVDD18_IORT
ANT_SEL1	DIO	Antenna select 1	DVDD18_IORT
ANT_SEL2	DIO	Antenna select 2	DVDD18_IORT

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Pin name	Type	Description	Power domain
BSI			
RFIC_MIPI0_SCLK	DIO	RFIC0 MIPI CLK	DVDD18_IOBR
RFIC_MIPI0_SDATA	DIO	RFIC0 MIPI DATA	DVDD18_IOBR
RFIC_MIPI1_SCLK	DIO	RFIC1 MIPI CLK	DVDD18_IOBR
RFIC_MIPI1_SDATA	DIO	RFIC1 MIPI DATA	DVDD18_IOBR
RFIC_MIPI2_SCLK	DIO	RFIC2 MIPI CLK	DVDD18_IOBL
RFIC_MIPI2_SDATA	DIO	RFIC2 MIPI DATA	DVDD18_IOBL
RFIC_MIPI3_SCLK	DIO	RFIC3 MIPI CLK	DVDD18_IOBL
RFIC_MIPI3_SDATA	DIO	RFIC3 MIPI DATA	DVDD18_IOBL
RFIC0_BSI_CK	DIO	RFIC0 BSI CLK	DVDD18_IOBL
RFIC0_BSI_D0	DIO	RFIC0 BSI DATA0	DVDD18_IOBL
RFIC0_BSI_D1	DIO	RFIC0 BSI DATA1	DVDD18_IOBL
RFIC0_BSI_D2	DIO	RFIC0 BSI DATA2	DVDD18_IOBL
RFIC0_BSI_EN	DIO	RFIC0 BSI CS	DVDD18_IOBL
MSDC0			
MSDC0_DAT7	DIO	MSDC0 data7 pin	DVDD18_MC0
MSDC0_DAT6	DIO	MSDC0 data6 pin	DVDD18_MC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	DVDD18_MC0
MSDC0_RSTB	DIO	MSDC0 reset output	DVDD18_MC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	DVDD18_MC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	DVDD18_MC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	DVDD18_MC0
MSDC0_CMD	DIO	MSDC0 command pin	DVDD18_MC0
MSDC0_CLK	DIO	MSDC0 clock output	DVDD18_MC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	DVDD18_MC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	DVDD18_MC0
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	DVDD28_MC1/DVDD18_MC1
MSDC1_CMD	DIO	MSDC1 command pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT0	DIO	MSDC1 data0 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT1	DIO	MSDC1 data1 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT2	DIO	MSDC1 data2 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT3	DIO	MSDC1 data3 pin	DVDD28_MC1/DVDD18_MC1
WiFi/BT/GPS			
WB_SDATA	DIO	WiFi/BT SPI control data	DVDD18_IORT
WB_SCLK	DIO	WiFi/BT SPI control clock	DVDD18_IORT
WB_SEN	DIO	WiFi/BT SPI control enable	DVDD18_IORT
WB_RSTB	DIO	WiFi/BT SPI control reset	DVDD18_IORT
F2W_CLK	DIO	FM clock	DVDD18_IORT
F2W_DATA	DIO	FM data	DVDD18_IORT
WB_CTRL0	DIO	Data bus 0	DVDD18_CONN
WB_CTRL1	DIO	Data bus 1	DVDD18_CONN
WB_CTRL2	DIO	Data bus 2	DVDD18_CONN

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Pin name	Type	Description	Power domain
WB_CTRL3	DIO	Data bus 3	DVDD18_CONN
WB_CTRL4	DIO	Data bus 4	DVDD18_CONN
WB_CTRL5	DIO	Data bus 5	DVDD18_CONN
EFUSE			
FSOURCE_P	DIO	E-FUSE blowing power control	FSOURCE_P
EMI			
EMI0_CK_C	DIO	DRAM clock 0 output	AVDDQ_EMI0_0
EMI0_CK_T	DIO	DRAM clock 0 output #	AVDDQ_EMI0_0
EMI0_CKE0	DIO	DRAM command output CKE	AVDDQ_EMI0_0
EMI0_CS0_N	DIO	DRAM chip select 0 #	AVDDQ_EMI0_0
EMI0_CS1_N	DIO	DRAM chip select 1 #	AVDDQ_EMI0_0
EMI0_CA0	DIO	DRAM address output 0	AVDDQ_EMI0_0
EMI0_CA1	DIO	DRAM address output 1	AVDDQ_EMI0_0
EMI0_CA2	DIO	DRAM address output 2	AVDDQ_EMI0_0
EMI0_CA3	DIO	DRAM address output 3	AVDDQ_EMI0_0
EMI0_CA4	DIO	DRAM address output 4	AVDDQ_EMI0_0
EMI0_CA5	DIO	DRAM address output 5	AVDDQ_EMI0_0
EMI0_CA6	DIO	DRAM address output 6	AVDDQ_EMI0_0
EMI0_CA7	DIO	DRAM address output 7	AVDDQ_EMI0_0
EMI0_CA8	DIO	DRAM address output 8	AVDDQ_EMI0_0
EMI0_CA9	DIO	DRAM address output 9	AVDDQ_EMI0_0
EMI0_DM0	DIO	DRAM DQM 0	AVDDQ_EMI0_0
EMI0_DM1	DIO	DRAM DQM 1	AVDDQ_EMI0_0
EMI0_DM2	DIO	DRAM DQM 2	AVDDQ_EMI0_0
EMI0_DM3	DIO	DRAM DQM 3	AVDDQ_EMI0_0
EMI0_DQS0_C	DIO	DRAM DQS 0	AVDDQ_EMI0_0
EMI0_DQS0_T	DIO	DRAM DQS 0 #	AVDDQ_EMI0_0
EMI0_DQS1_C	DIO	DRAM DQS 1	AVDDQ_EMI0_0
EMI0_DQS1_T	DIO	DRAM DQS 1 #	AVDDQ_EMI0_0
EMI0_DQS2_C	DIO	DRAM DQS 2	AVDDQ_EMI0_0
EMI0_DQS2_T	DIO	DRAM DQS 2 #	AVDDQ_EMI0_0
EMI0_DQS3_C	DIO	DRAM DQS 3	AVDDQ_EMI0_0
EMI0_DQS3_T	DIO	DRAM DQS 3 #	AVDDQ_EMI0_0
EMI0_DQ0	DIO	DRAM data pin 0	AVDDQ_EMI0_0
EMI0_DQ1	DIO	DRAM data pin 1	AVDDQ_EMI0_0
EMI0_DQ2	DIO	DRAM data pin 2	AVDDQ_EMI0_0
EMI0_DQ3	DIO	DRAM data pin 3	AVDDQ_EMI0_0
EMI0_DQ4	DIO	DRAM data pin 4	AVDDQ_EMI0_0
EMI0_DQ5	DIO	DRAM data pin 5	AVDDQ_EMI0_0
EMI0_DQ6	DIO	DRAM data pin 6	AVDDQ_EMI0_0
EMI0_DQ7	DIO	DRAM data pin 7	AVDDQ_EMI0_0
EMI0_DQ8	DIO	DRAM data pin 8	AVDDQ_EMI0_0
EMI0_DQ9	DIO	DRAM data pin 9	AVDDQ_EMI0_0

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Pin name	Type	Description	Power domain
EMI0_DQ10	DIO	DRAM data pin 10	AVDDQ_EMI0_0
EMI0_DQ11	DIO	DRAM data pin 11	AVDDQ_EMI0_0
EMI0_DQ12	DIO	DRAM data pin 12	AVDDQ_EMI0_0
EMI0_DQ13	DIO	DRAM data pin 13	AVDDQ_EMI0_0
EMI0_DQ14	DIO	DRAM data pin 14	AVDDQ_EMI0_0
EMI0_DQ15	DIO	DRAM data pin 15	AVDDQ_EMI0_0
EMI0_DQ16	DIO	DRAM data pin 16	AVDDQ_EMI0_0
EMI0_DQ17	DIO	DRAM data pin 17	AVDDQ_EMI0_0
EMI0_DQ18	DIO	DRAM data pin 18	AVDDQ_EMI0_0
EMI0_DQ19	DIO	DRAM data pin 19	AVDDQ_EMI0_0
EMI0_DQ20	DIO	DRAM data pin 20	AVDDQ_EMI0_0
EMI0_DQ21	DIO	DRAM data pin 21	AVDDQ_EMI0_0
EMI0_DQ22	DIO	DRAM data pin 22	AVDDQ_EMI0_0
EMI0_DQ23	DIO	DRAM data pin 23	AVDDQ_EMI0_0
EMI0_DQ24	DIO	DRAM data pin 24	AVDDQ_EMI0_0
EMI0_DQ25	DIO	DRAM data pin 25	AVDDQ_EMI0_0
EMI0_DQ26	DIO	DRAM data pin 26	AVDDQ_EMI0_0
EMI0_DQ27	DIO	DRAM data pin 27	AVDDQ_EMI0_0
EMI0_DQ28	DIO	DRAM data pin 28	AVDDQ_EMI0_0
EMI0_DQ29	DIO	DRAM data pin 29	AVDDQ_EMI0_0
EMI0_DQ30	DIO	DRAM data pin 30	AVDDQ_EMI0_0
EMI0_DQ31	DIO	DRAM data pin 31	AVDDQ_EMI0_0
EMI0_EXTR	DIO	DRAM REXTDN pin	AVDDQ_EMI0_0
VREF_EMI0	DIO		AVDDQ_EMI0_0
CAM			
CMPCLK	DIO	Pixel clock from sensor	DVDD18_IORT
CMMCLK0	DIO	Master clock0 to sensor	DVDD18_IORB
CMMCLK1	DIO	Master clock1 to sensor	DVDD18_IORT
CMDAT0	DIO	CAM sensor Data0	DVDD18_IORT
CMDAT1	DIO	CAM sensor Data1	DVDD18_IORT
I2C0			
I2C0_SCL	DIO	I2C0 clock	DVDD18_IORB
I2C0_SDA	DIO	I2C0 data	DVDD18_IORB
I2C1			
I2C1_SCL	DIO	I2C1 clock	DVDD18_IORB
I2C1_SDA	DIO	I2C1 data	DVDD18_IORB
I2C2			
I2C2_SCL	DIO	I2C2 clock	DVDD18_IORB
I2C2_SDA	DIO	I2C2 data	DVDD18_IORB
I2C3			
I2C3_SCL	DIO	I2C3 clock	DVDD18_IORB
I2C3_SDA	DIO	I2C3 data	DVDD18_IORB
ABB			

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Pin name	Type	Description	Power domain
DET_BBIN	AIO	PAD_DET_BBIN	AVDD18_MD
DET_BBIP	AIO	PAD_DET_BBIP	AVDD18_MD
DET_BBQN	AIO	PAD_DET_BBQN	AVDD18_MD
DET_BBQP	AIO	PAD_DET_BBQP	AVDD18_MD
DRX_BB_IN	AIO	PAD_DRX_BB_IN	AVDD18_MD
DRX_BB_IP	AIO	PAD_DRX_BB_IP	AVDD18_MD
DRX_BB_QN	AIO	PAD_DRX_BB_QN	AVDD18_MD
DRX_BB_QP	AIO	PAD_DRX_BB_QP	AVDD18_MD
LTEX26M_IN	AIO	26MHz clock input for AP and modem	AVDD18_MD
PRX_BB_IN	AIO	PAD_PRX_BB_IN	AVDD18_MD
PRX_BB_IP	AIO	PAD_PRX_BB_IP	AVDD18_MD
PRX_BB_QN	AIO	PAD_PRX_BB_QN	AVDD18_MD
PRX_BB_QP	AIO	PAD_PRX_BB_QP	AVDD18_MD
TX_BBIN	AIO	PAD_TX_BBIN	AVDD18_MD
TX_BBIP	AIO	PAD_TX_BBIP	AVDD18_MD
TX_BBQN	AIO	PAD_TX_BBQN	AVDD18_MD
TX_BBQP	AIO	PAD_TX_BBQP	AVDD18_MD
APC	AIO	Automatic power control for modem	AVDD18_MD
AUXIN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUXIN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUXIN2	AIO	AuxADC external input channel 2	AVDD18_AP
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
AVSS_REFN	GND	Negative reference port for internal circuit	AVDD18_AP
WBG			
XIN_WBG	AIO	WIFI/BT clock source	AVDD18_WBG
GPS_RXQN	AIO	RXQN for GPS RX	AVDD18_WBG
GPS_RXQP	AIO	RXQP for GPS RX	AVDD18_WBG
GPS_RXIN	AIO	RXIN for GPS RX	AVDD18_WBG
GPS_RXIP	AIO	RXIP for GPS RX	AVDD18_WBG
WB_TXQN	AIO	TXQN for WIFI/BT TX	AVDD18_WBG
WB_TXQP	AIO	TXQP for WIFI/BT TX	AVDD18_WBG
WB_TXIN	AIO	TXIN for WIFI/BT TX	AVDD18_WBG
WB_TXIP	AIO	TXIP for WIFI/BT TX	AVDD18_WBG
WB_RXQN	AIO	RXQN for WIFI/BT RX	AVDD18_WBG
WB_RXQP	AIO	RXQP for WIFI/BT RX	AVDD18_WBG
WB_RXIN	AIO	RXIN for WIFI/BT RX	AVDD18_WBG
WB_RXIP	AIO	RXIP for WIFI/BT RX	AVDD18_WBG
MIPI			
TDN3	AIO	DSI0 lane3 N	AVDD18_MIPITX
TDP3	AIO	DSI0 lane3 P	AVDD18_MIPITX

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Pin name	Type	Description	Power domain
TDN2	AIO	DSI0 lane2 N	AVDD18_MIPITX
TDP2	AIO	DSI0 lane2 P	AVDD18_MIPITX
TCN	AIO	DSI0 CK lane N	AVDD18_MIPITX
TCP	AIO	DSI0 CK lane P	AVDD18_MIPITX
TDN1	AIO	DSI0 lane1 N	AVDD18_MIPITX
TDP1	AIO	DSI0 lane1 P	AVDD18_MIPITX
TDN0	AIO	DSI0 lane0 N	AVDD18_MIPITX
TDP0	AIO	DSI0 lane0 P	AVDD18_MIPITX
VRT	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground	AVDD18_MIPITX
RDN3	AIO	CSI0 lane3 N	AVDD18_MIPIRX0
RDP3	AIO	CSI0 lane3 P	AVDD18_MIPIRX0
RDN2	AIO	CSI0 lane2 N	AVDD18_MIPIRX0
RDP2	AIO	CSI0 lane2 P	AVDD18_MIPIRX0
RCN	AIO	CSI0 CK lane N	AVDD18_MIPIRX0
RCP	AIO	CSI0 CK lane P	AVDD18_MIPIRX0
RDN1	AIO	CSI0 lane1 N	AVDD18_MIPIRX0
RDP1	AIO	CSI0 lane1 P	AVDD18_MIPIRX0
RDN0	AIO	CSI0 lane0 N	AVDD18_MIPIRX0
RDP0	AIO	CSI0 lane0 P	AVDD18_MIPIRX0
RDN1_A	AIO	CSI1 lane1 N	AVDD18_MIPIRX1
RDP1_A	AIO	CSI1 lane1 P	AVDD18_MIPIRX1
RCN_A	AIO	CSI1 CK lane N	AVDD18_MIPIRX1
RCP_A	AIO	CSI1 CK lane P	AVDD18_MIPIRX1
RDN0_A	AIO	CSI1 lane0 N	AVDD18_MIPIRX1
RDP0_A	AIO	CSI1 lane0 P	AVDD18_MIPIRX1
RDN2_A	AIO	CSI1 lane 2 N	AVDD18_MIPIRX1
RDP2_A	AIO	CSI1 lane 2 P	AVDD18_MIPIRX1
RDN3_A	AIO	CSI1 lane 3 N	AVDD18_MIPIRX1
RDP3_A	AIO	CSI1 lane 3 P	AVDD18_MIPIRX1
USB			
USB_DP	AIO	USB port0 D+ differential data line	AVDD33_USB
USB_DM	AIO	USB port0 D- differential data line	AVDD33_USB
CHD_DP	AIO	BC1.2 Charger DP	AVDD33_USB
CHD_DM	AIO	BC1.2 Charger DM	AVDD33_USB
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
Keypad			
KPROW0	AIO	Keypad row 0	DVDD18_IOBR
KPROW1	AIO	Keypad row 1	DVDD18_IOBR
KPROW2	AIO	Keypad row 2	DVDD18_IOBR

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Pin name	Type	Description	Power domain
KPCOL0	AIO	Keypad column 0	DVDD18_IOBR
KPCOL1	AIO	Keypad column 1	DVDD18_IOBR
KPCOL2	AIO	Keypad column 2	DVDD18_IOBR
Analog power			
AVDD18_PLLGP	P	Analog power input 1.8V for PLL	
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX, 2GBBTX	
AVDD18_USB	P	Analog power 1.8V for USB	
AVDD18_WBG	P	Analog power 1.8V for WiFi/BT/GPS	
AVDD18_MIPITX	P	Analog power for MIPI DSI	
AVDD18_MIPIRX0	P	Analog power for MIPI CSI	
AVDD18_MIPIRX1	P	Analog power for MIPI CSI	
AVDD33_USB	P	Analog power 3.3V for USB port 1	
Digital power			
DVDD18_IOBL	P	Digital power input for IO	-
DVDD18_IOBR	P	Digital power input for IO	-
DVDD18_IOLT	P	Digital power input for IO	-
DVDD18_IORB	P	Digital power input for IO	
DVDD18_IORT	P	Digital power input for IO	
DVDD18_IR	P	Digital power input for IO	
DVDD28_IR_DVDD18_EINT	P	Digital power input for 1.8/3.3V IO	
DVDD18_CONN	P	Digital power input for IO	-
EVDD18_EFUSE	P	Digital power input for efuse IO	-
DVDD18_MC0	P	Digital power input for MSDC0 IO	-
DVDD18_MC1	P	Digital power input for MSDC1 IO	-
DVDD28_MC1	P	Digital power input for 1.8/3.3V MSDC IO	-
DVDD28_SIM1	P	Digital power input for SIM1	
DVDD28_SIM2	P	Digital power input for SIM2	
DVDD_TOP	P	Digital power input for core	-
DVDD_MODEM	P	Digital power input for LTE	-
DVDD_TOP_SRAM	P	Digital power input for LTE and core SRAM	-
DVDD_DVFS	P	Digital power input for processor	-
DVDD_DVFS_SRAM	P	Digital power input for processor SRAM	-
AVDDQ_EMI0_0	P	Digital power input for DDR	
AVDDQ_EMI0_1	P	Digital power input for DDR	
AVDDQ_EMI0_2	P	Digital power input for DDR	
AVDDQ_EMI0_3	P	Digital power input for DDR	
VREF_EMI0	P	Digital power input for DDR	

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Pin name	Type	Description	Power domain
Analog ground			
AVSS18_AP	G	Analog ground	
AVSS18_MD	G	Analog ground	
AVSS18_PLLGP	G	Analog ground	
AVSS18_WBG	G	Analog ground	
AVSS_REFN	G	Analog ground	
AVSS33_USB	G	Analog ground	
DVSS18_MIPITX	G	Analog ground	
DVSS18_MIPIRX0	G	Analog ground	
DVSS18_MIPIRX1	G	Analog ground	
Digital ground			
DVSS	G	Digital ground	-

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-4. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
AVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.9	V
AVDD18_MIPITX	Analog power for MIPI DSI	1.7	1.9	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI- & CSI1	1.7	1.9	V
AVDD33_USB_P	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.7	1.9	V
DVDD18_CONN DVDD18_IOBL DVDD18_IOBR DVDD18_IOLT DVDD18_IORB DVDD18_IORT DVDD18_IR DVDD18_MC0 DVDD18_MC1	Digital power input for 1.8V IO	1.62	1.98	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.98	V
DVDD18_MC1	Digital power input for MSDC1	1.62	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	3.6	V
DVDD28_SIM1	Digital power input for SIM1	1.7	3.3	V
DVDD28_SIM2	Digital power input for SIM2	1.7	3.3	V
DVDD18_EFUSE	Digital power for EFUSE	1.8	2.2	V
AVDDQ_EMI0_0 AVDDQ_EMI0_1 AVDDQ_EMI0_2 AVDDQ_EMI0_3	Digital power input for DRAM	1.14	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.746	1.31	V
DVDD_DVFS_SRAM	Digital power input for DVFS SRAM	0.746	1.31	
DVDD_MODEM	Digital power input for LTE	0.746	1.294	V
DVDD_TOP_SRAM	Digital power input for SRAM	0.746	1.294	V
DVDD_TOP (DVDD_CORE)	Digital power input for TOP	0.746	1.294	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

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2.2.2 Recommended Operating Conditions

Table 2-5. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.8	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.8	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.8	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
AVDD18_MIPITX1	Analog power for MIPI DSI	1.7	1.8	1.9	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI	1.7	1.8	1.89	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
DVDD18_CONN DVDD18_IOBL DVDD18_IOBR DVDD18_IOLT DVDD18_IORB DVDD18_IORT DVDD18_IR DVDD18_MC0 DVDD18_MC1	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.8	1.98	V
DVDD18_MC1	Digital power input for MSDC1	1.62	1.8	1.98	V
DVDD28_MC1	Digital power input for MSDC1	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7	3.0	3.3	V
		1.7	1.8	1.9	
DVDD18_EFUSE	Digital power for EFUSE	1.8	2	2.2	V
AVDDQ_EMI0_0 AVDDQ_EMI0_1 AVDDQ_EMI0_2 AVDDQ_EMI0_3	Digital power input for EMI (LPDDR2/3)	1.14	1.2	1.3	V
DVDD_DVFS (DVDD_CPU)	Digital power input for DVFS	0.746	1.15	1.31	V
DVDD_DVFS_SRAM	Digital power input for DVFS SRAM	0.746	1.15	1.31	
DVDD_LTE	Digital power input for LTE	0.746	1.15	1.294	V
DVDD_TOP_SRAM	Digital power input for SRAM	0.746	1.15	1.294	V
DVDD_TOP (DVDD_CORE)	Digital power input for TOP	0.746	1.15	1.294	V

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2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1 External Memory Interface for LPDDR3

The external memory interface, shown in Figure 2-2. Basic timing parameter for LPDDR3 commands, Figure 2-3 and Figure 2-4, is used to connect LPDDR3 device for MT6739CH. It includes pins CLK_T, CLK_C, CKE[1:0], CS[1:0], DQS[3:0], DQS#[3:0], CA[9:0] and DQ[31:0]. Table 2-6 summarizes the symbol definition and the related timing specifications.

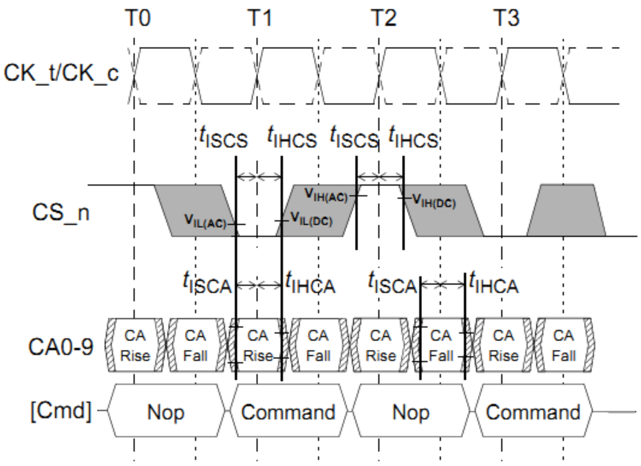

Figure 2-2. Basic timing parameter for LPDDR3 commands

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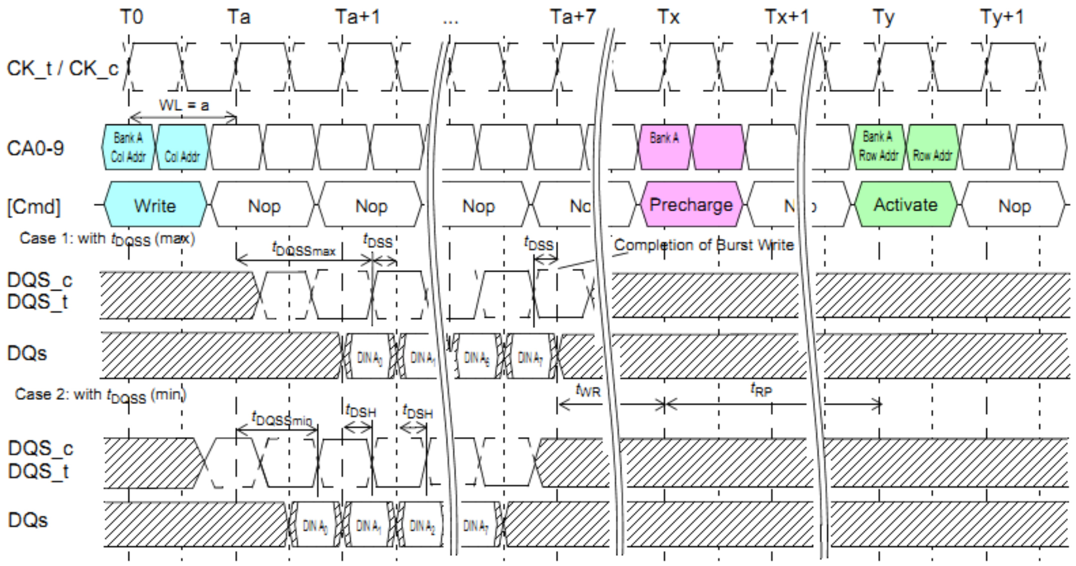

Figure 2-3. Basic timing parameter for LPDDR3 write

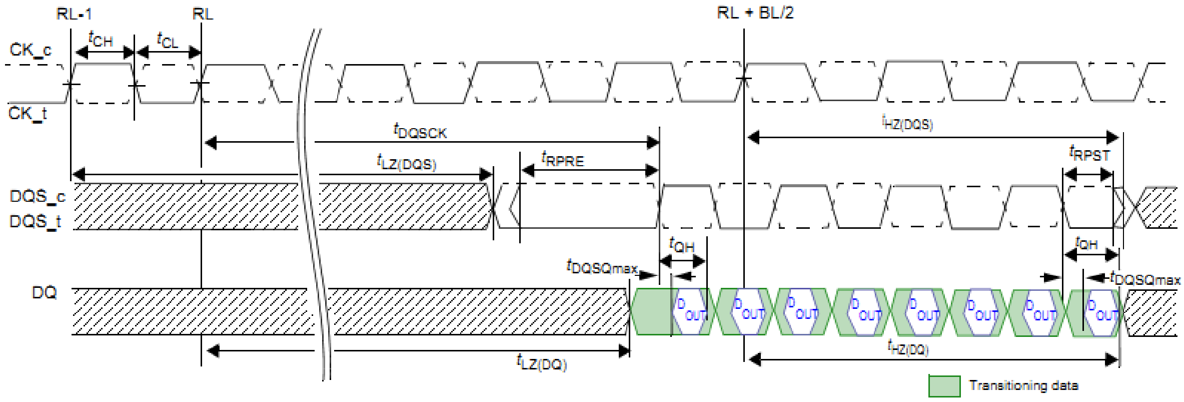

Figure 2-4. Basic LPDDR3 read timing parameter

Table 2-6. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	1.071		100	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.13			ns
tDH	DQ & DM input hold time	0.13			ns
tDIPW	DQ and DM input pulse width	0.35			tCK
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK

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Symbol	Description	Min.	Typ.	Max.	Unit
tDSH	DQS falling edge hold time from CK	0.2			tCK
tWPST	Write postamble	0.4			tCK
tWPRE	Write preamble	0.8			tCK
tISCA	Address & control input setup time	0.13			ns
tIHCA	Address & control input hold time	0.13			ns
tISCS	CS_ input setup time	0.23			ns
tIHCS	CS_ input hold time	0.23			ns
tIPWCA	Address and control input pulse width	0.35			tCK
tIPWCS	CS_ input pulse width	0.7			tCK
tCKE	CKE minimum pulse width (HIGH and LOW pulse width)	Max. (7.5ns, 3tCK)			ns
tISCKE	CKE input setup time	0.25			tCK
tIHCKE	CKE input hold time	0.25			tCK
tCPDED	Command path disable delay	2			tCK
tLZ(DQS)	DQS low-impedance time from CK/CK’	tDQSCK (MIN) - 0.3			ns
tHZ(DQS)	DQS high-impedance time from CK/CK’			tDQSCK (MAX) – 0.1	ns
tLZ(DQ)	DQ low-impedance time from CK/CK’	tDQSCK (MIN) - 0.3			ns
tHZ(DQ)	DQ high-impedance time from CK/CK’			tDQSCK (MAX) + [1.4*tDQSQ (MAX)]	ns
tDQSQ	DQS-DQ skew			0.115	ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tQH	DQ/DQS output hold time from DQS	Min. (tQSH, tQSL)			ns
tMRW	MODE register Write command period	Max. (10tCK, 15)			ns
tMRR	MODE register Read command period	4			tCK
tMRD	Mode register set command delay	Max. (10tCK, 14)			ns
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	Max. (42ns, 3tCK)		70000	ns
tRC	ACTIVE to ACTIVE command period	tRAS + tRPab (with all-bank pre-charge) tRAS + tRPpb (with per-bank pre-			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
		charge)			
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			ns
tRCD	ACTIVE to READ or WRITE delay	Max. (18ns, 3tCK)			ns
tRPpb	Row PRECHARGE Time (single bank)	Max. (18ns, 3tCK)			ns
tRPab	Row PRECHARGE Time (all banks)	Max. (21ns, 3tCK)			ns
tRRD	ACTIVE bank A to ACTIVE bank B delay	Max. (10ns, 2tCK)			ns
tWR	WRITE recovery time	Max. (15ns, 4tCK)			ns
tWTR	Internal write to READ command time	Max. (7.5ns, 4tCK)			ns
tXSR	SELF REFRESH exit to next valid command	Max. (tRFCab + 10ns, 2tCK)			ns
tXP	EXIT power down to next valid command delay	Max. (7.5ns, 3tCK)			ns
tREFW	Refresh period			32	ms
tRFCab	Refresh cycle time	130			ns
tRFCpb	Per bank refresh cycle time	60			ns
tRTP	Internal READ to PRECHARGE command delay	Max. (7.5ns, 4tCK)			ns
tCCD	CAS-to-CAS delay	4			tCK

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-7. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_DAT_MOSI [1] PWRAP_SPI0_CSN	00: No dedicate JTAG 01: No dedicate JTAG 10: No dedicate JTAG (default) 11: Use CAM pins for legacy JTAG
AUD_DAT_MISO1[0] ANT_SEL2[1]	00: eMMC Boot (default) 01: N.A 10: TLC Boot 11: SLC Boot
PWRAP_SPI0_MO[0] PWRAP_SPI0_MI[1]	00: LP3/LP2 (default) 01: N.A 10: N.A 11: N.A

2.3.2 Constant Tie Pins

Table 2-8. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

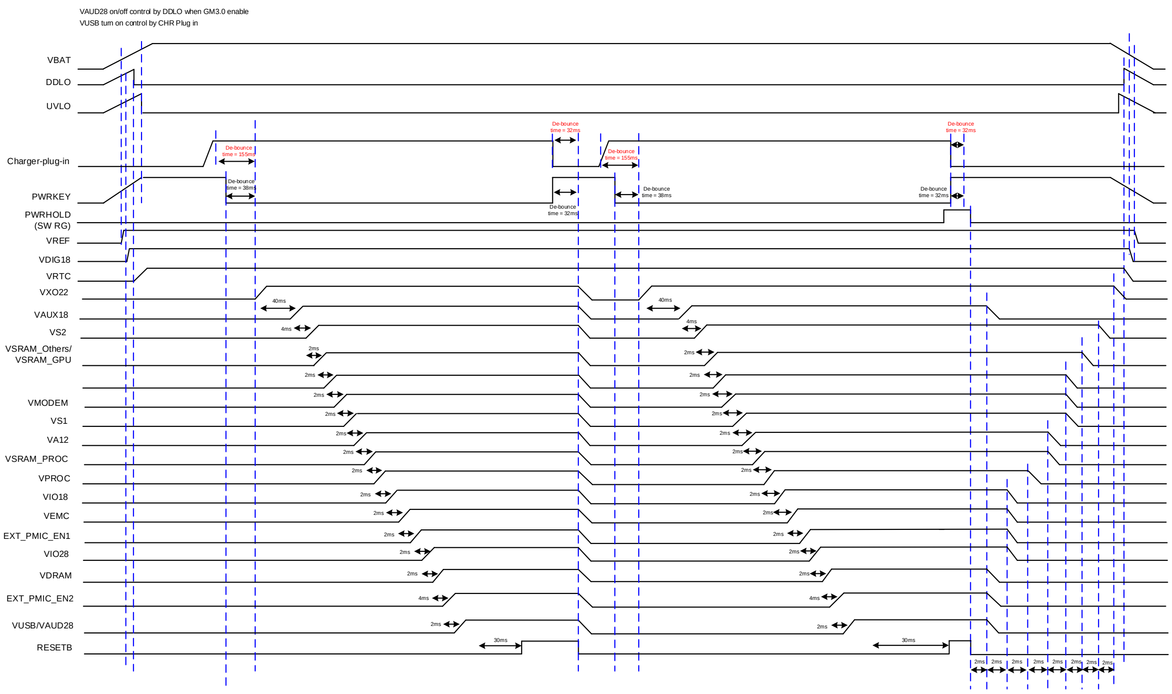

Figure 2-5. Power on/off sequence by pressing PWRKEY

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- DPDADC: ADC output for BBTX digital predistortion technique.
- RF control: DAC for automatic power control (APC) is included.The output is provided to external RF power amplifier.
- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 13 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- LTE_BBRX
- LTE_BBTX
- DPDADC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 LTE_BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.

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2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

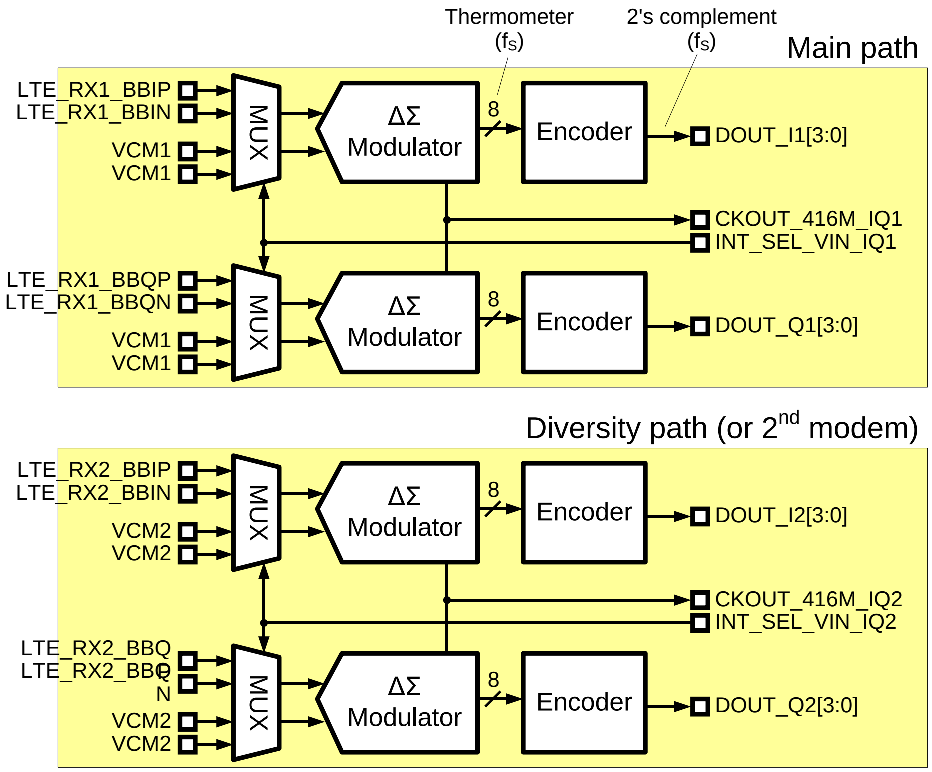

Figure 2-6. Block diagram of LTE_BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-9. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency – Clock rate (LTE HB mode) – Clock rate (LTE LB mode) – Clock rate (DC mode) – Clock rate (SC mode & GSM mode)		208 208 208 208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, DC mode			0.14	% (rms)

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)
RIN	Differential input resistance – LTE HB mode – LTE LB mode – DC mode – SC mode & GSM mode	 6.3 6.3 6.3 6.3	 9 9 9 9	 11.7 11.7 11.7 11.7	kΩ
FS	Output sampling rate		208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – LTE HB mode, 2.4Vpp (10.2MHz) sinewave, 1kHz ~ 9MHz band – LTE LB mode, 2.4Vpp (5.2MHz) sinewave, 1kHz ~ 4.5MHz band – DC mode, 2.4Vpp (5.2MHz) sinewave, 400kHz ~ 4.6MHz band – SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band – GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	70 73 73 76 83	72 75 75 78 86		dB dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	–20		80	°C
	Current consumption (per channel, 1 ADC) – Power-up – Power-down			 3 10	 mA uA

2.5.3.2 LTE_BBTX

2.5.3.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

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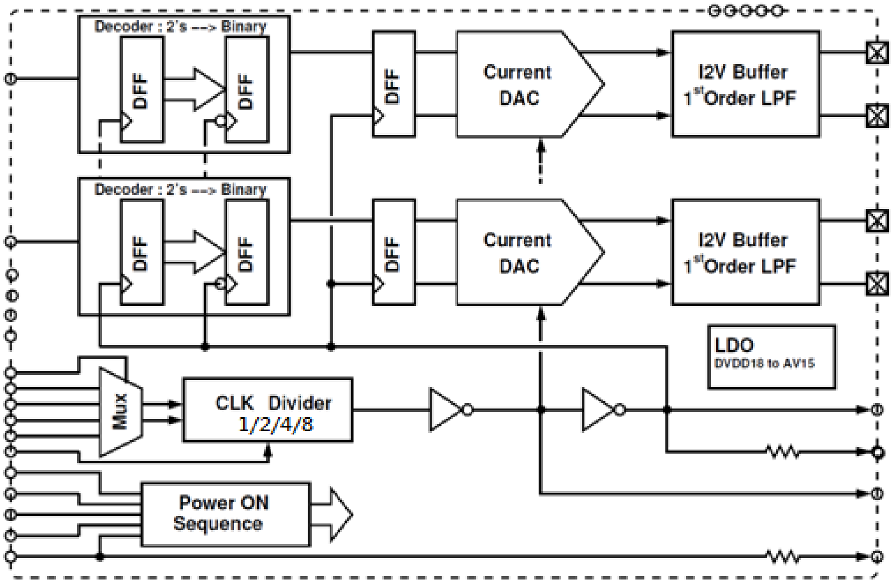

Figure 2-7. Block diagram of LTE_BBTX

2.5.3.2.2 Functional Specifications

Table 2-10. LTE_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF leakage current @ supply, Irms @416*2 = 832MHz			3.5	uA
V_{fs}	DAC output swing		2000		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock – LTE mode – 3G, TD mode		 416 104		MHz
I_{mis}	1-sigma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
N_{OOB}	Output noise level @25MHz		40		nVrms/sqrt(Hz)
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test – 2G Mode – 3G Talking Mode – LTE 1CA 20M		 -65 -55 -58	 -62 -52 -55	 dBc dBc dBc
T	Operating temperature	-20		80	°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Current consumption – Power-up – Power-down		 6.5 10		 mA uA

2.5.3.3 DPDADC

2.5.3.3.1 Block Descriptions

The DPDADC (Digital Pre-Distortion ADC) helps to control the spectral re-growth and more TX power can be transmitted without violating the spectral mask. The DPD ADC includes:

1. I/Q Channel Buffer between input and ADC.
2. I/Q Channel 10-Bit ADC with 1.2Vdpp input Range.

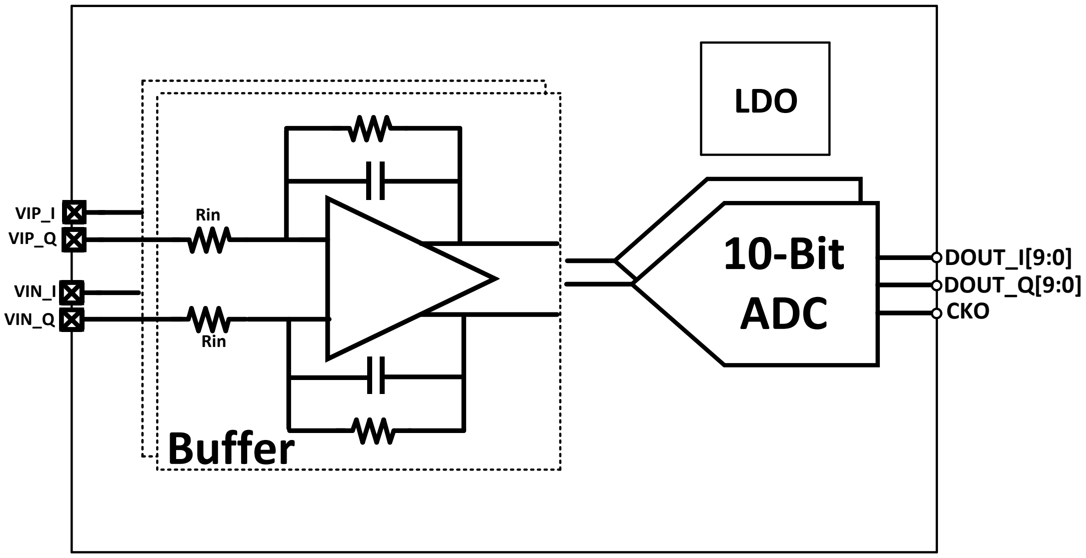

Figure 2-8. Block diagram of DPDADC

2.5.3.3.2 Functional Specfications

Table 2-11. DPDADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	ADC input Range	1.15	1.2	1.25	Vdpp
Bits	ADC Bits Number		10		Bit
Fs	ADC sampling frequency		208		MHz
DR	0~Fs/2		52		dB
IM3	0.6V, 8M&9M input		-66	-63	dBc
VCM IN	Input common-mode Voltage		0.55		V
V_{os}	Input referred Offset (3-Sigma)		20	30	mV

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Symbol	Parameter	Min.	Typ.	Max.	Unit
I/Q Phase mismatch	I/Q Phase mismatch		1.5	2	Deg
I/Q Gain mismatch	I/Q Gain mismatch		0.2	0.3	dB
Gain Drift	Gain Drift over -20 to 120 degree.			0.3	dB
I/Q Isolation	I/Q cross talk at 9M			-55	dB
Rin	Input resistor	3.2	4	4.8	KΩ
Cin	Input capacitance		2	3	pF
Buffer isolation	Buffer isolation @ 104MHz (ADC to buffer input)	-100			dB
Leakage	Current Leakage to supply			10	uA/Hz
Settling time			3	5	us
AVDD	Analog power supply	1.7	1.8	1.9	V
DVDD	Digital power supply	-5%	1.15	+5%	V
T	Operating temperature	-20		120	°C
I_{ON}	Current consumption			6	mA

2.5.3.4 APC-DAC

2.5.3.4.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

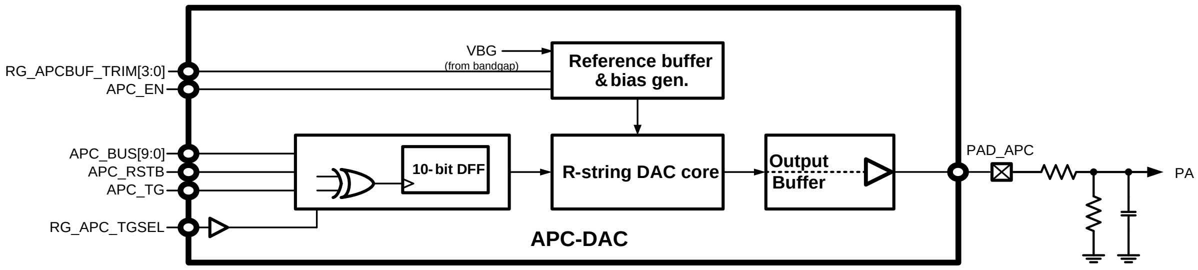

Figure 2-9. Block diagram of APC-DAC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-12. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s

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Symbol	Parameter	Min.	Typ.	Max.	Unit
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		450		uA
I_{OFF}	Current consumption (power-down state)			20	uA

2.5.3.5 AUXADC

2.5.3.5.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

See Table 2-13 for brief descriptions of AUXADC input channels.

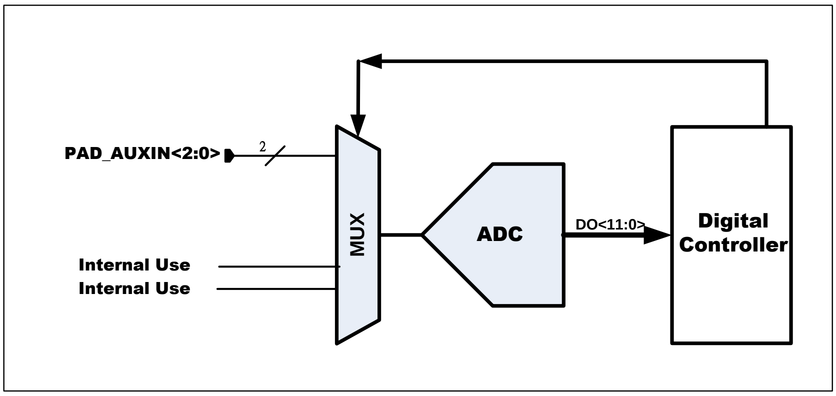

Figure 2-10. Block diagram of AUXADC

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Table 2-13. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	NA
Channel 3	NA
Channel 4	NA
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	Internal use
Channel 11	Internal use
Channel 12	External use (AUX_IN2)
Channel 13	NA
Channel 14	NA
Channel 15	NA

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-14. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		3.25/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel		 50 4		 fF pF
RIN	Input resistance Unselected channel	 20			 MΩ
	Clock latency		N+8		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 1.0833MHz clock rate)	56	64		dB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Current consumption - Power-up - Power-down		 600 1		 uA uA
	Accuracy- before trim			+-45	mV
	Accuracy- after trim			+-10	mV

2.5.3.6 Clock Squarer

2.5.3.6.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-15. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		500		uA

2.5.3.7 Phase Locked Loop

2.5.3.7.1 Block Descriptions

There are total 12 PLLs in PLL macro, providing several clocks for CPU, BUS, modem, analog modem, MSDC and image-sensor.

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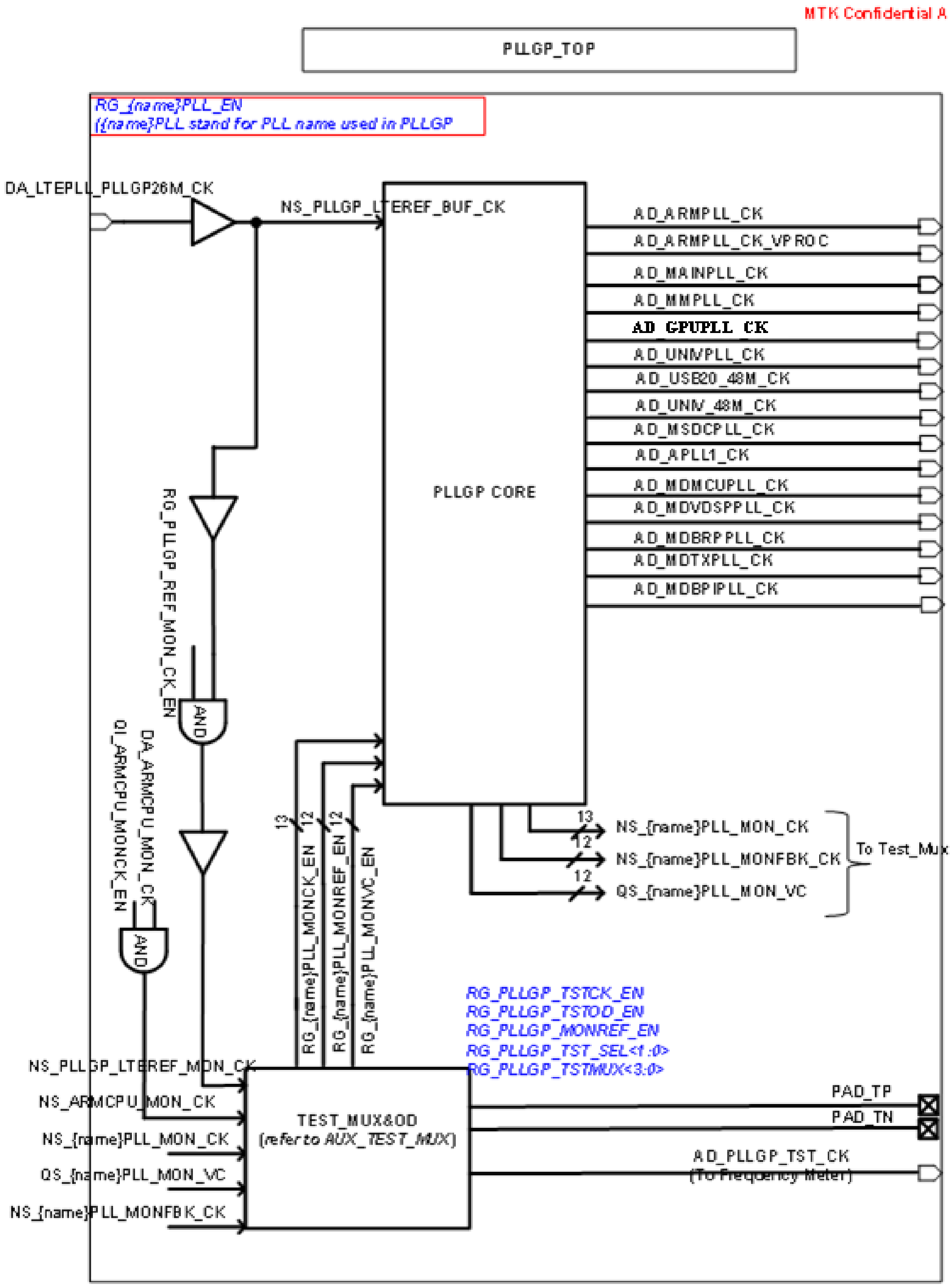

Figure 2-11. Block diagram of PLLGP

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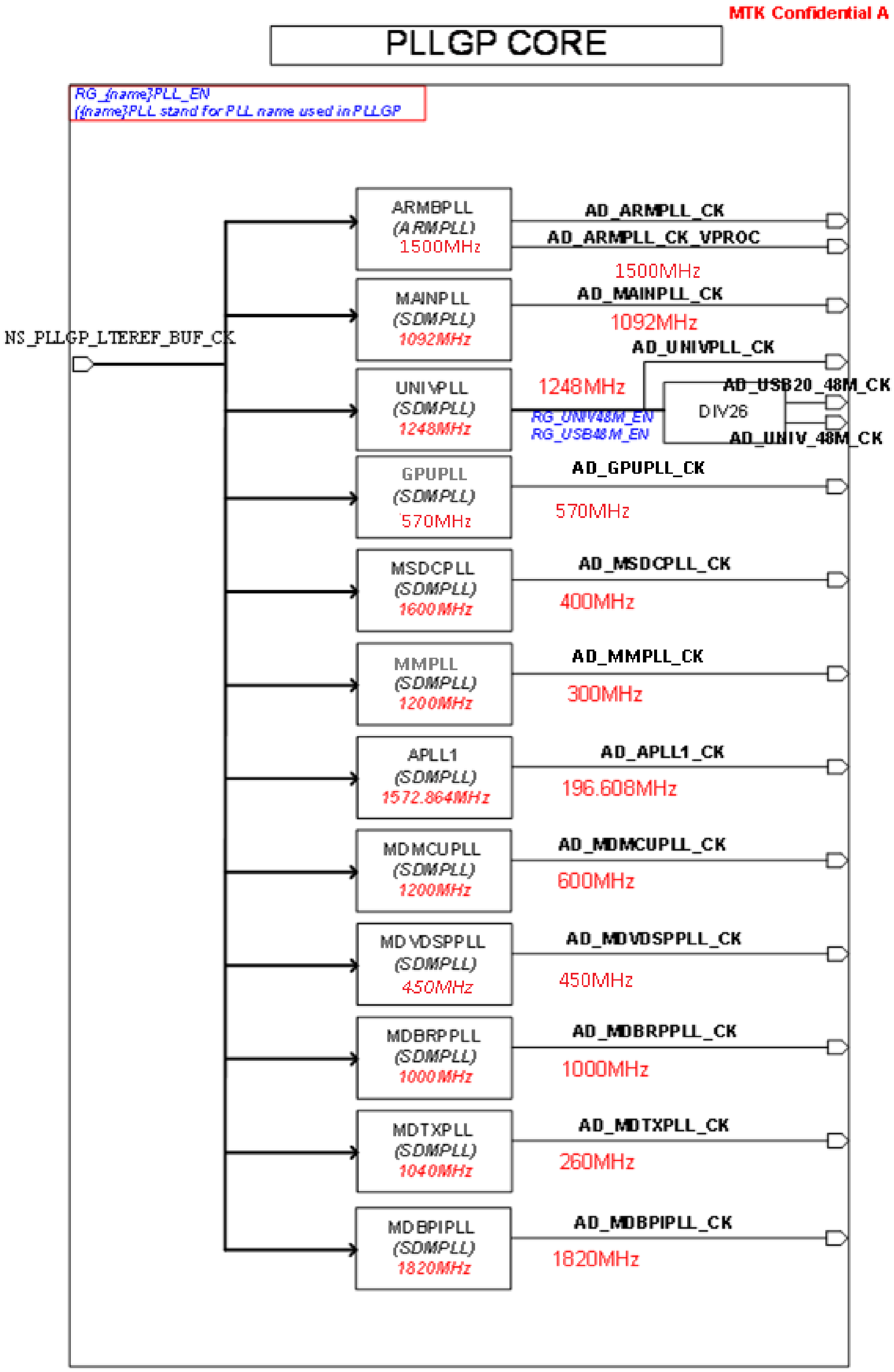

Figure 2-12. Block diagram of PLLGP CORE

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2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of PLL.

Table 2-16. ARMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1500		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			1	uA

Table 2-17. MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1092		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			1	uA

Table 2-18. GPUPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		570		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

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Table 2-19. UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	1248	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-20. MSDCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		400		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-21. MMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		300		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

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Table 2-22. APLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		196.608		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-23. MDMCUPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		600		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-24. MDVDSPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		450		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

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Table 2-25. MDBRPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1000		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-26. MDTXPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		260		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-27. MDBPIPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1820		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

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2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-28. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		12		uA

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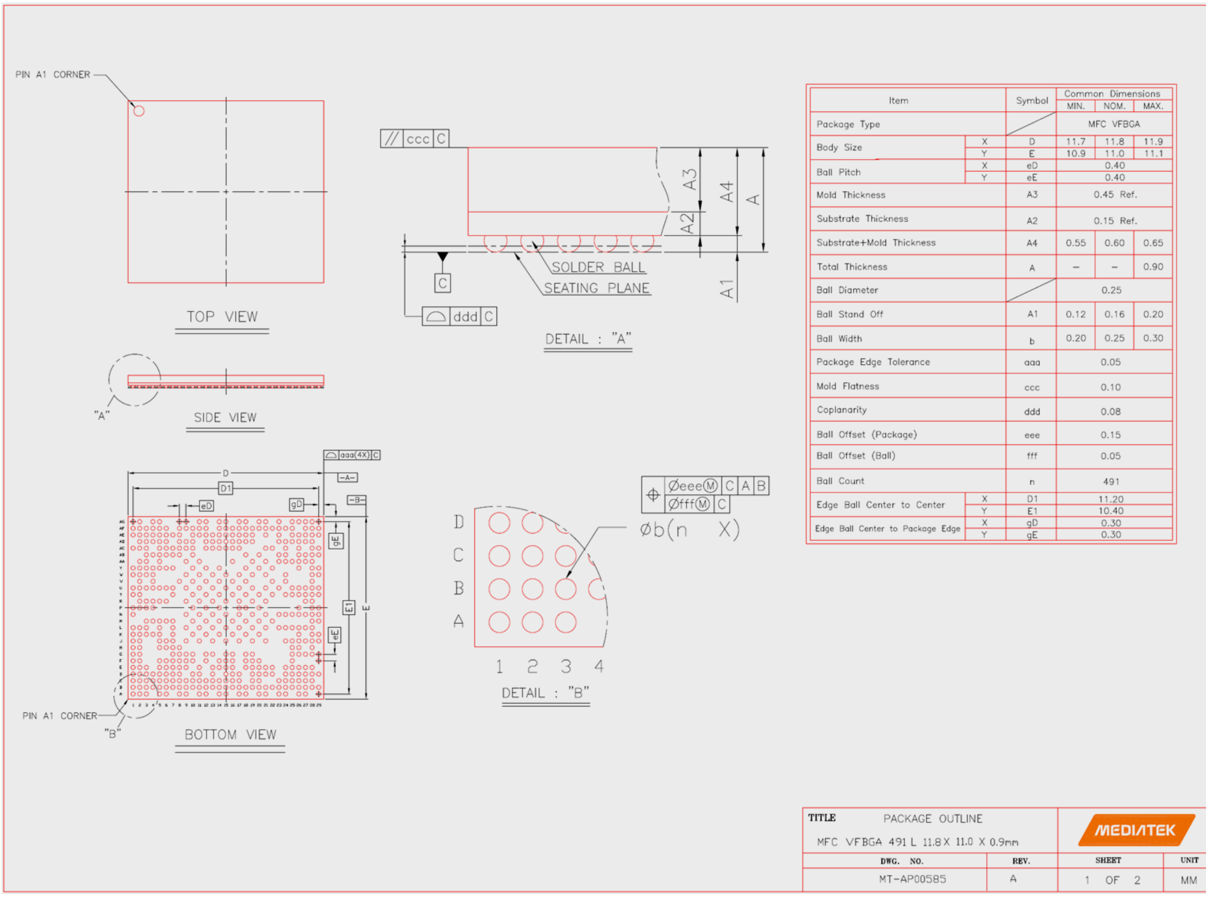
2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	11.7	11.8	11.9
	Y	E	10.9	11.0	11.1
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.15 Ref.		
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	491		
Edge Ball Center to Center	X	D1	11.20		
	Y	E1	10.40		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

Figure 2-13. Outlines and dimensions of VFBGA 11.8mm*11.0mm, 491 balls, 0.4mm pitch package

2.6.2 Thermal Operating Specifications

Table 2-29. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection		°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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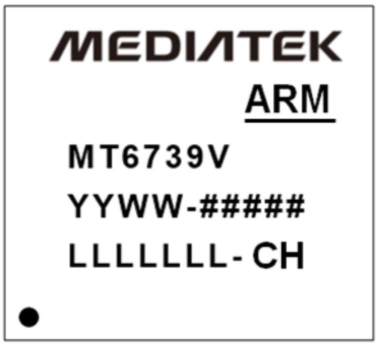
2.7 Ordering Information

2.7.1 Top Marking Definition



- YYWW: Date code
- %: Functional code
- #####: Internal control code
- LLLLLLL: Die lot No.

Figure 2-14. Top marking of MT6739CH

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